

SEMICONDUCTOR DEVICE HAVING REDUCED CAPACITANCE TO SUBSTRATE
AND METHOD

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Abstract of the Disclosure

10 In one embodiment, a matrix of free-standing
semiconductor shapes are oxidized to form a low capacitance
isolation tub. The adjacent rows of shapes in the matrix
are offset with respect to each to minimize air gap and void
formation during tub formation. In a further embodiment,
the spacing between adjacent rows is less than the spacing
15 between shapes within a row.